


# PATENT COOPERATION TREATY

## PCT

### INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 03/064 WO	<b>FOR FURTHER ACTION</b>		See Form PCT/IPEA/416
International application No. PCT/CH2004/000691	International filing date (day/month/year) 16.11.2004	Priority date (day/month/year) 17.11.2003	
International Patent Classification (IPC) or national classification and IPC H01L29/10, H01L29/739, H01L21/331			
Applicant ABB TECHNOLOGY AG			
<p>1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.</p> <p>2. This REPORT consists of a total of 12 sheets, including this cover sheet.</p> <p>3. This report is also accompanied by ANNEXES, comprising:</p> <p>a. <input checked="" type="checkbox"/> sent to the applicant and to the International Bureau) a total of 1 sheets, as follows:</p> <p><input type="checkbox"/> sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).</p> <p><input checked="" type="checkbox"/> sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.</p> <p>b. <input type="checkbox"/> (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).</p>			
<p>4. This report contains indications relating to the following items:</p> <p><input checked="" type="checkbox"/> Box No. I Basis of the opinion</p> <p><input type="checkbox"/> Box No. II Priority</p> <p><input type="checkbox"/> Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability</p> <p><input type="checkbox"/> Box No. IV Lack of unity of invention</p> <p><input checked="" type="checkbox"/> Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement</p> <p><input type="checkbox"/> Box No. VI Certain documents cited</p> <p><input type="checkbox"/> Box No. VII Certain defects in the international application</p> <p><input checked="" type="checkbox"/> Box No. VIII Certain observations on the international application</p>			
Date of submission of the demand  27.05.2005		Date of completion of this report  28.12.2005	
Name and mailing address of the international preliminary examining authority:  European Patent Office - P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk - Pays Bas Tel. +31 70 340 - 2040 Tx: 31 651 epo nl Fax: +31 70 340 - 3016		Authorized Officer  Franche, V  Telephone No. +31 70 340-4998	



# INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.  
PCT/CH2004/000691

## Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.
  - ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
    - ☐ international search (under Rules 12.3 and 23.1(b))
    - ☐ publication of the international application (under Rule 12.4)
    - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)
2. With regard to the **elements\*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report):*

### Description, Pages

1-9 as originally filed

### Claims, Numbers

2-5 as originally filed

1 as amended (together with any statement) under Art. 19 PCT

### Drawings, Sheets

1/4-4/4 as originally filed

☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
  - ☐ the description, pages
  - ☐ the claims, Nos.
  - ☐ the drawings, sheets/figs
  - ☐ the sequence listing (*specify*):
  - ☐ any table(s) related to sequence listing (*specify*):
4. ☒ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
  - ☐ the description, pages
  - ☒ the claims, Nos. 1
  - ☐ the drawings, sheets/figs
  - ☐ the sequence listing (*specify*):
  - ☐ any table(s) related to sequence listing (*specify*):

\* If item 4 applies, some or all of these sheets may be marked "superseded."

**INTERNATIONAL PRELIMINARY REPORT  
ON PATENTABILITY**

International application No.  
PCT/CH2004/000691

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**Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

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1. Statement

Novelty (N)	Yes: Claims	1-5
	No: Claims	
Inventive step (IS)	Yes: Claims	
	No: Claims	1-5
Industrial applicability (IA)	Yes: Claims	1-5
	No: Claims	

2. Citations and explanations (Rule 70.7):

**see separate sheet**

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**Box No. VIII Certain observations on the international application**

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The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

**see separate sheet**

**Re Item I**

**Basis of the report**

The amendment filed with the International Bureau under Article 19(1) introduces subject-matter which extends beyond the content of the application as filed, contrary to Article 19(2) PCT. The amendment concerned is the following: a top metallization layer 9 "being contacted by one or more source regions 6" (see line 28 in claim 1).

The applicant wrote in the letter dated 16-03-2005 that new claim 1 is based on original claim 1, Figure 1 and description, page 5, lines 24-25.

However, it is written in the description, page 5, lines 24-25 that "base region 82 laterally does not extend or overlaps the two source regions 6". There is therefore not suggestion that the metallization layer 9 is contacted by one or more source regions 6.

Furthermore, the applicant cited Figure 1, where the metallization layers 9 is contacted by one or more source regions 6, but this is only one of the features disclosed by this figure. It is not derivable from Figure 1 that this new feature can be isolated from the other features shown in Figure 1.

The amendment in claim 1 is therefore not directly and unambiguously derivable from the application as filed.

Claim 1 is thus not allowable.

**Re Item V**

**Reasoned statement with regard to novelty, inventive step or industrial applicability;  
citations and explanations supporting such statement**

1. Reference is made to the following documents:

- D1: US-A-4 896 196 (BLANCHARD RICHARD A ET AL) 23 January 1990 (1990-01-23)  
D2: US-A-5 451 531 (TOMOMATSU YOSHIFUMI ET AL) 19 September 1995 (1995-09-19)  
D3: US-A-4 443 931 (ADLER MICHAEL S ET AL) 24 April 1984 (1984-04-24)  
D4: US-A-5 703 383 (NAKAYAMA KAZUYA) 30 December 1997 (1997-12-30)  
D5: EP-A-1 227 522 (TOKYO SHIBAURA ELECTRIC CO) 31 July 2002 (2002-07-31)

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-5 does not involve an inventive step in the sense of Article 33(3) PCT.

- 2.1 Document D1, which is considered to represent the most relevant state of the art, discloses (see figures 1 and 3a; the references in parentheses applying to this document):

an insulated gate bipolar transistor, comprising:

a N- type semiconductor substrate (52);

a P+ type drain layer (51);

a P type channel layer (20);

N+ type source layers (32, 34);

a first supplementary P+ type region (21) overlapping the channel region and a part of the substrate (52).

From which the subject-matter of claim 1 differs in that there is another supplementary region of P type conductivity that encompasses the source regions.

The problem to be solved by the present invention may be regarded as preventing the latch-up phenomenon.

The solution proposed in claim 1 of the present application cannot be considered as involving an inventive step (Articles 52(1) and 56 EPC) for the following

reasons:

An IGBT with another supplementary region of P type conductivity that encompasses the source regions is described in document D2 (see figure 3) as preventing the latch-up phenomenon. The skilled person would therefore regard it as a normal design option to include this feature in the IGBT described in document D1 in order to solve the problem posed.

The subject-matter of claim 1 is therefore not inventive.

- 2.2 Dependent claims 2 and 3 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, meet the requirements of the EPC with respect to inventive step, the reasons being as follows.

Document D3 (see figure 14, column 4, line 57 - line 68; the references in parentheses applying to this document) discloses an insulated gate bipolar transistor whose the depth of the supplementary P+ region (28) exceeds by at least a factor of 1.5 the depth of the P type channel region (34).

The problem may be regarded as increasing the breakdown voltage.

The person skilled in the art would form a supplementary P+ region whose the depth exceeds by at least a factor of 1.5 the depth of the P type channel region as in document D3 in order to increase the breakdown voltage.

The subject-matter of claim 2 is therefore not inventive.

The person skilled in the art would use an impurity concentration at least 5 times higher than the doping concentration of the channel layer because the higher the impurity concentration, the better the hole collection and therefore the higher the performances of the device.

The subject-matter of claim 3 is therefore not inventive.

INTERNATIONAL PRELIMINARY  
REPORT ON PATENTABILITY  
(SEPARATE SHEET)

International application No.

PCT/CH2004/000691

- 2.3 Document D4 (see column 5, line 6 - line 42, column 8, line 5 - line 14 and figure 2; the references in parentheses applying to this document) discloses a IGBT with

Two supplementary regions (8) of N-type conductivity  
in the vicinity of the channel region.

t  
w  
o  
s  
u  
p  
p  
l  
e  
m  
e  
n  
t  
a  
r  
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e  
g  
i  
o  
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9  
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o  
f  
N  
-  
t

**INTERNATIONAL PRELIMINARY  
REPORT ON PATENTABILITY  
(SEPARATE SHEET)**

International application No.

PCT/CH2004/000691

y  
p  
e  
c  
o  
n  
d  
u  
c  
t  
i  
v  
i  
t  
y  
i  
n  
t  
h  
e  
v  
i  
c  
i  
n  
i  
t  
y  
o  
f  
t  
h  
e  
c



h  
a  
n  
n  
e  
l  
r  
e  
g  
i  
o  
n

The problem may be regarded as lowering the on-voltage of the device.

The person skilled in the art would have added these two supplementary regions to an IGBT as disclosed in document D4 in order to lower the on-voltage of the *device*

d  
e  
v  
i  
c  
e

The subject-matter of claim 4 is therefore not inventive.

- 2.4 Document D5 (see paragraphs 62 - 64 and figure 14; the references in parentheses applying to this document) describes an IGBT with a gate insulating film made of many portions (21a and 21b), the first portion (21a) having a thickness smaller than the other portion (21b).

The problem may be regarded as obtaining a smaller capacitance between the gate

**INTERNATIONAL PRELIMINARY  
REPORT ON PATENTABILITY  
(SEPARATE SHEET)**

International application No.

PCT/CH2004/000691

and the drain.

The person skilled in the art would have formed an IGBT with a gate insulating film made of different portions with different thicknesses as disclosed in document D5

*in order to obtain a smaller capacitance between the gate and the drain.*

i  
n  
o  
r  
d  
e  
r  
t  
o  
o  
b  
t  
a  
i  
n  
a  
s  
m  
a  
l  
l  
e  
r  
c  
a  
p  
a  
c  
i  
t

**INTERNATIONAL PRELIMINARY  
REPORT ON PATENTABILITY  
(SEPARATE SHEET)**

International application No.

PCT/CH2004/000691

a  
n  
c  
e  
b  
e  
t  
w  
e  
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n  
t  
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r  
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n  
.

The subject-matter of claim 5 is therefore not inventive.

**Re Item VIII**

**Certain observations on the international application**

1. The application does not meet the requirements of Article 6 PCT, because claims 1 and 4 are not clear.
  - 1.1 It is said in claim 1 that the base region (81) does not adjoin the second main surface underneath the gate oxide layer.  
The expression "second main surface" in claim 1 is not clear because the first main surface has not been defined. ✓  
Moreover, it is said in the description (see page 5, lines 5-6) that the base region (81) does not adjoin the top surface underneath the gate oxide film (41) which is not consistent with the figure 1 where the base region (81) adjoins the surface underneath the gate oxide film.  
It is therefore absolutely not clear either in the claims or in the description what the "second main surface" is.  
This feature is therefore disregarded in the communication.
  - 1.2 In claim 1, the impurity concentration of the two base regions (81 and 82) is not specified. It could therefore be the same as the channel region (7) and in that case the base regions (81 and 82) would not be distinguishable from the channel region (7). ✓
  - 1.3 Claim 4 is not consistent with the description because the protection region (3) adjoins the top surface of the substrate (2) in figure 5 and the bottom surface of the substrate in claim 4. ✓

The subject-matter of claims 1 and 4 is therefore not clear.

IAP9 Rec'd PCT/PTO 17 MAY 2006

**NEW PATENT CLAIM**

1. An insulated gate bipolar transistor, comprising

- a semiconductor substrate (2) having a top and a bottom surface, a gate insulation film (41) formed on the top surface, said gate insulation film (41) comprising at least one contact opening,
- said semiconductor substrate (2) comprising
  - an emitter layer (21) of first conductivity type adjoining said bottom surface,
  - a drift region (22) of second conductivity type adjoining said emitter layer (21),
  - a channel region (7) of first conductivity type formed in the drift region (22) underneath the contact opening and underneath part of the gate insulation film (41),
  - one or more source regions (6) of second conductivity type disposed in the channel region (7) and delimiting a base contact area (821);
- a gate electrode (5) formed on the gate insulation film (41),
- a bottom metallization layer (1) formed on the bottom surface,
- a top metallization layer (9) covering the contact opening and being contacted by one or more source regions (6),

characterized in that

- a first base region (81) of first conductivity type is disposed in the channel region (7) so that it encompasses the one or more source regions (6), but does not adjoin the second main surface underneath the gate oxide layer (41), and in that
- a second base region (82) of first conductivity type is confined in the semiconductor substrate (2) to a region underneath the base contact area (821) so that it partially overlaps with the channel region (7) and with the first base region (81).